AMENDMENTS TO THE CLAIMS

1. (**Currently amended**) A semiconductor processing tool comprising:

a first substrate handling chamber;

a front docking port located on an outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station directly adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates;

wherein the robot arm is configured to access the buffer station.

2. (**Original**) The semiconductor processing tool according to Claim 1, wherein the rack is configured to support a plurality of 300 mm silicon wafers.

3. (**Original**) The semiconductor processing tool according to Claim 1, further comprising a rear substrate handling chamber, where the loadlock chamber is located between the first substrate handling chamber and the rear substrate handling chamber.

4. (**Original**) The semiconductor processing tool according to Claim 1, wherein the buffer station is further configured to create an inert environment which is selectively isolated from the first substrate handling chamber.

5. (**Original**) The semiconductor processing tool according to Claim 4, wherein the buffer station is further configured to be selectively purged.

6. (**Original**) The semiconductor processing tool according to Claim 4, wherein the buffer station rack is configured to allow the robot arm to be capable of accessing the entire buffer station rack through the use of a z-motion of the robot arm.

7. (**Original**) The semiconductor processing tool according to Claim 1, wherein the buffer station is configured to have a internal volume less than or equal to about 18.3 liters.

8. (**Original**) The semiconductor processing tool according to Claim 7, wherein the buffer station rack is configured to support twenty-five 300 mm silicon wafers.

9. (**Previously Presented**) The semiconductor processing tool according to Claim 1, wherein the loadlock chamber is configured to have an internal volume less than or equal to about 9.156 liters.

10. (**Currently amended**) A semiconductor processing tool comprising:

a first substrate handling chamber;

a front docking port located on the outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station directly adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates, wherein the shelves of the buffer station rack have a reduced pitch relative to shelves of a front opening unified pod (FOUP) for the same size substrates;

wherein the robot arm is configured to access the buffer station.

11. (**Currently amended**) The semiconductor processing tool according to Claim 10, wherein the robot arm is configured to employ a variable pitch end effector having multiple end effector shelves.

12. (**Currently amended**) The semiconductor processing tool according to Claim 10, wherein the first substrate handling chamber is configured to operate at atmospheric pressure.

13. (**Currently amended**) The semiconductor processing tool according to Claim 10, wherein the first substrate handling chamber is configured to operate at reduced pressure.

14. (**Currently amended**) A semiconductor processing tool comprising:

a substrate handling chamber;

a front docking port located on an outside surface of the substrate handling chamber, the port being capable of mating with a cassette;

a cassette rack internal to the docked cassette;

a purgeable buffer station joined with ~~and adjacent~~ the substrate handling chamber such that it is possible to transfer substrates directly between the substrate handling

chamber and the buffer station, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber, the buffer station being located in position downstream of the front docking port, the buffer station having only one opening for substrate transfer to and from the buffer station; and

a buffer station rack within the buffer station being configured to have multiple slots for holding substrates.

15. **(Original)** The semiconductor processing tool according to Claim 14, further comprising a loadlock chamber joined with the substrate handling chamber, the loadlock chamber having a loadlock rack with a substrate capacity of less than one third of a substrate capacity of the cassette.

16. **(Original)** The semiconductor processing tool according to Claim 15, further comprising a rear substrate handling chamber where the loadlock chamber is located between the substrate handling chamber and the rear substrate handling chamber.

17. **(Original)** The semiconductor processing tool according to Claim 15, wherein the substrate capacity of the loadlock chamber is 1 to 7 substrates.

18. **(Original)** The semiconductor processing tool according to Claim 15, wherein the loadlock rack is configured to support a plurality of 300 mm silicon wafers.

19. **(Original)** The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at standard atmospheric pressure.

20. **(Original)** The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at reduced pressure.

21. **(Original)** The semiconductor processing tool according to Claim 14, wherein the buffer station rack has a reduced relative spacing between the rack slots as compared with a relative spacing between slots of the cassette.

22. **(Original)** The semiconductor processing tool according to Claim 14, wherein the buffer station rack is a reduced pitch rack configured to allow a robot arm to be capable of accessing the entire buffer station rack through the use of a robot arm's z-motion.

23. **(Original)** The semiconductor processing tool according to Claim 14, further comprising a robot arm configured to have a variable pitch end effector designed to transfer

multiple substrates from the cassette rack to the buffer station rack, the cassette rack having unequal slot pitch relative to the buffer station rack.